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EXAMINER	
CHANDRASEKHAR, PRANAV	
ART UNIT	PAPER NUMBER
2115	2

DATE MAILED: 04/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/847,975	KIM, JASON SEUNG-MIN	
	Examiner	Art Unit	
	Pranav Chandrasekhar	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 May 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-51* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-51* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 7,25 and 40 are objected to because of the following informalities:

In line 3 of claims 7,25 and 40, the three clocks are referred to as being "independently and simultaneously" thus rendering the claim to be incomplete. For examination purposes, the clocks are viewed as being independently and simultaneously generated.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1 and 19 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Kohara [US Pat No. 6,600,575].

3. As per claim 1, Kohara teaches

a clock generator circuit for generating one or more different clock signals wherein each clock signal has a different predetermined frequency [10 and C1 Fig 1;

col. 4 lines 37-42. The designated but different frequencies are viewed as being predetermined.];

a clock selector circuit [12 and 13 Fig 1] that, based on the task being performed by the computer system, dynamically adjusts the clock signal supplied to each component of the computer system in order to reduce the total power being consumed by the computer system [col. 5 line 63- col. 6 line 5; col. 6 lines 33-64].

4. As per claim 19, Kohara teaches

simultaneously generating one or more different clock signals wherein each clock signal has a different predetermined frequency [col. 10 and C1 Fig 1; col. 4 lines 37-42. The designated but different frequencies are viewed as being predetermined.];

dynamically adjusts the clock signal supplied to each component of the computer system in order to reduce the total power being consumed by the computer system [col. 5 line 63- col. 6 line 5; col. 6 lines 33-64].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 4,12-18,22,30-37 and 45-51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kohara [US Pat No. 6,600,575] in view of Mensch Jr. [US Pat No. 5,737,613].

6. As per claim 37, Kohara teaches a clock select circuit [13 Fig 1] that selects one of a first, second and third clock signal that is supplied to a portion of the computer system [col. 6 lines 33-64].

Kohara does not explicitly teach

a first oscillator that generates a first clock signal;

a second clock oscillator that generates a second clock signal; and

a programmable clock circuit that generates a third clock signal based on the second clock signal;

Mensch Jr teaches

a first oscillator that generates a first clock signal [359 Fig 1H; col. 12 lines 57-64];

a second clock oscillator that generates a second clock signal [351 Fig 1H; col. 12 lines 38-43]; and

a programmable clock circuit that generates a third clock signal based on the second clock signal [365 Fig 1H; col. 12 lines 44-49].

It would have been obvious to one skilled in the art to combine the teachings of Kohara and Mensch Jr to provide two separate clock oscillators outputting two clock signals wherein a third clock signal is derived from the faster oscillator and to select one of the three clock signals to be supplied to a portion of a computer system depending on the appropriate clock speed required because the three clock signals signify a high speed clock signal, a clock signal with a speed in between the high speed and low speed (the third clock signal) and a low speed clock signal. It would be advantageous to

have each of these signals readily available to be supplied to a portion of the computer system based on the need of that particular portion.

7. As per claims 4 and 22, Kohara does not explicitly teach a clock generator circuit comprising a first oscillator that generates a first clock signal, a second clock oscillator that generates a second clock signal and a programmable clock circuit that generates a third clock signal based on the second clock signal.

Mensch Jr. teaches

a first oscillator that generates a first clock signal [359 Fig 1H; col. 12 lines 57-64];

a second clock oscillator that generates a second clock signal [351 Fig 1H; col. 12 lines 38-43]; and

a programmable clock circuit that generates a third clock signal based on the second clock signal [365 Fig 1H; col. 12 lines 44-49].

It would have been obvious to one skilled in the art to combine the teachings of Kohara and Mensch Jr. to provide two separate clock oscillators outputting two clock signals wherein a third clock signal is derived from the faster oscillator and to select one of the three clock signals to be supplied to a portion of a computer system depending on the appropriate clock speed required because the three clock signals signify a high speed clock signal, an clock signal with a speed in between the high and low speed (the third clock signal) and a low speed clock signal. It would be advantageous to have each of these signals readily available to be supplied to a portion of the computer system based on the need of that particular portion.

8. As per claims 12,30 and 45, Kohara and Mensch Jr do not explicitly teach the programmable clock circuit generating a fourth clock signal.

It would have been obvious to one skilled in the art to modify the teachings of Kohara and Mensch Jr to enable the programmable clock circuit to generate a fourth clock signal.

9. As per claims 13,31 and 46, Kohara and Mensch Jr do not explicitly teach the first, second, third and fourth clock signals having different frequencies.

It would have been obvious to one skilled in the art to modify the teachings of Kohara and Mensch Jr to enable the first, second, third and fourth clock signals to have different frequencies.

10. As per claims 14,32 and 47, Kohara and Mensch Jr do not explicitly teach the first clock signal comprising 32 kHz, the second clock signal comprising 24 MhZ, the third clock signal frequency comprising 33 MhZ and the fourth clock signal frequency comprising 66 MhZ.

It would have been obvious to one skilled in the art to modify the teachings of Kohara and Mensch Jr to designate 32 kHz to the first clock signal, 24 MhZ to the second clock signal, 33 MhZ to the third clock signal and 66 MhZ to the fourth clock signal.

11. As per claims 16, 34 and 49, Kohara further teaches the clock select circuit means for dynamically changing the clock frequency applied to each component of the computer system based on the task being performed by the computer system [col. 5 line 63- col. 6 line 5; col. 6 lines 33-64].

12. As per claims 17,35 and 50, Kohara and Mensch Jr do not explicitly teach the clock select circuit comprising a multiplexer.

It would have been obvious to one skilled in the art to modify the teachings of Kohara and Mensch Jr to incorporate a multiplexer within the clock supply circuit since the function of a multiplexer is to select one signal from a plurality of signals on the basis of received selector signals.

13. As per claims 18,36 and 51, Kohara and Mensch Jr do not explicitly teach the programmable clock generator further comprising a prescalar unit and a post scalar unit whose outputs are fed into a phase locked loop that generates a third clock signal and a fourth clock signal having different frequencies.

It would have been obvious to one skilled in the art to modify the teachings of Kohara and Mensch Jr to enable the programmable clock generator to comprise a prescalar unit and a post scalar unit whose outputs are fed into a phase locked loop that generates a third clock signal and a fourth clock signal having different frequencies.

14. As per claims 15, 33 and 48, Kohara and Mensch Jr do not explicitly teach a time of day circuit that generates time of day clock signals based on the first clock signal.

It would have been obvious to one skilled in the art to modify the teachings of Kohara and Mensch Jr to incorporate a time of day circuit that generates time of day clock signals based on the first clock signal since the time of the system must be maintained.

15. Claims 5-11,23-29 and 38-44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kohara [US Pat No. 6,600,575] in view of Mensch Jr [US Pat No. 5,737,613] as applied to claim 37 above, and further in view of Lin et al [US Pat No. 6,163,583].

16. As per claims 5,23 and 38, Kohara and Mensch Jr do not explicitly teach a clock state machine for detecting a clock state of the computer system at a predetermined time and a clock policy circuit for generating control signals to the control select circuit in order to output the appropriate clock signal.

Lin teaches a clock state machine for determining a clock state of the computer system and a clock policy circuit for generating control signals to a control select circuit in order to output the appropriate clock signal [col. 8 lines 6-13.The clock state is viewed as being determined as a result of receiving the external access signal.].

Lin does not explicitly teach determining a clock state at a predetermined time.

It would have been obvious to one skilled in the art to combine the teachings of Kohara, Mensch Jr and Lin to incorporate a clock state machine to determine the state in response to which a clock policy circuit generates control signals to the control select circuit in order to output the appropriate clock signal since it would be advantageous to determine clock frequency on the basis of the state of the computer system. Furthermore, it would have been obvious to extend the teachings of Lin to execute the determination step at a predetermined time.

17. As per claims 6,24 and 39, Kohara, Mensch Jr and Lin do not explicitly teach the clock state machine comprising an idle state wherein the computer system is waiting

for an input, a busy state wherein the computer system is performing a task, a sleep state wherein the computer system has timed out due to inactivity and a dead state wherein power failed to the computer system.

It would have been obvious to one skilled in the art to modify the teachings of Mensch Jr, Kohara and Lin to incorporate states such as an idle state, busy state, sleep state and a dead state so as to determine the appropriate clock frequency associated with each of the states.

18. As per claims 7,25 and 40, Kohara, Mensch Jr and Lin do not explicitly teach a clock select circuit further comprising a circuit that generates a system clock, a circuit that generates a processor clock and a circuit that generates a co-processor clock wherein each of the clocks is independently and simultaneously generated.

It would have been obvious to one skilled in the art to modify the teachings of Kohara, Mensch Jr and Lin to incorporate circuits to independently and simultaneously generate a processor clock, a co-processor clock and system clock and hence make them readily available as opposed to deriving one clock from the other and increasing time delay of generation.

19. As per claims 8,26 and 41, Kohara, Mensch Jr and Lin do not explicitly teach during the idle state, the clock select circuit generating no clock for the phase locked loop and co-processor so that they are off, the clock select circuit generating the first clock signal for the processor so that the processor is clocked at a slow rate and the clock select circuit generating a high rate clock for an interrupt circuit so that the

interrupt circuit is active and can increase the clock frequency for the computer system quickly.

It would have been obvious to one skilled in the art to modify the teachings of Kohara, Mensch Jr and Lin to ensure that the clock select circuit generates no clock for the phase locked loop and processor in the idle state, generates the first clock signal for the processor so that the processor is clocked at a slow rate and generates a high rate clock for an interrupt circuit so that the interrupt circuit is active and can increase the clock frequency for the computer system quickly since the interrupts must be serviced and processed at a high rate, and the processor and phase locked loop are not crucial to the performance of the computer system in an idle state.

20. As per claims 9, 27 and 42, Kohara, Mensch Jr and Lin do not explicitly teach the clock select circuit generating a high rate clock signal for the processor, the co-processor and the interrupt circuits during the busy state.

It would have been obvious to one skilled in the art to modify the teachings of Kohara, Mensch Jr and Lin to enable the clock select circuit to generate a high rate clock signal for the processor, the co-processor and the interrupt circuits in the busy state, since in this state, the high speed of processing by the processor, co-processor and the interrupt circuits is crucial to the performance of the computer system.

21. As per claims 10,28 and 43, Kohara, Mensch Jr and Lin do not explicitly teach the clock select circuit generating no clock signal for the processor and the co-processor during the sleep state.

It would have been obvious to one skilled in the art to modify the teachings of Kohara, Mensch Jr and Lin to generate no clock signal for the processor and co-processor during the sleep state since no function is being performed by either of processors in the sleep state.

22. As per claims 11,29 and 44, Kohara, Mensch Jr and Lin do not explicitly teach the clock state machine being controlled by an interrupt signal and software commands.

It would have been obvious to one skilled in the art to modify the teachings of Kohara, Mensch Jr and Lin to enable the state machine to be controlled by an interrupt signal and software commands as they would dictate the appropriate clock speeds required for specific processes.

23. Claims 2,3,20 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kohara [US Pat No. 6,600,575] in view of Mustafa et al [US Pat No. 6,678,831].

24. As per claims 2 and 20, Kohara does not explicitly teach a static power management system wherein power is withdrawn from components that are not currently active to reduce the power consumption of the computer system.

Mustafa teaches power being withdrawn from components that are not currently active to reduce the power consumption of the computer system [col. 1 lines 10-19].

It would have been obvious to one skilled in the art to combine the teachings of Kohara and Mustafa to incorporate a static power management system wherein power

is removed from inactive components to further reduce the power consumed when no operation is being performed.

25. As per claims 3 and 21, Kohara and Mustafa do not explicitly teach a circuit for disconnecting the address, control data and data out pins of a component of the computer system in order to reduce the power consumption of the computer system.

It would have been obvious to one skilled in the art to modify the teachings of Kohara and Mustafa to disconnect the address, control data and data out pins of a component of the computer system since their operation is not required in an inactive state of the component.

Conclusion

26. An examination of this application reveals that applicant is unfamiliar with patent prosecution procedure. While an inventor may prosecute the application, lack of skill in this field usually acts as a liability in affording the maximum protection for the invention disclosed. Applicant is advised to secure the services of a registered patent attorney or agent to prosecute the application, since the value of a patent is largely dependent upon skilled preparation and prosecution. The Office cannot aid in selecting an attorney or agent.

Applicant is advised of the availability of the publication "Attorneys and Agents Registered to Practice Before the U.S. Patent and Trademark Office." This publication is for sale by the Superintendent of Documents, U.S. Government Printing Office, Washington, D.C. 20402.

27. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pranav Chandrasekhar whose telephone number is 703-305-8647. The examiner can normally be reached on 8:30 a.m.-5:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on 703-305-9717. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-7239 for regular communications and 703-746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-2100.

Pranav Chandrasekhar
March 31,2004

THOMAS LEE
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